REMARKS

Claims 1-20 are pending in this application. Claims 1-10 have been amended in several particulars for purposes of clarity and brevity that are unrelated to patentability and prior art rejections while Claims 11-20 have been newly added in accordance with current Office policy, to further and alternatively define Applicants' disclosed invention and to assist the Examiner to expedite compact prosecution of the instant application.

The title of the invention has been objected to for failing to sufficiently describe the invention. A new title of--SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD FOR HIGH RELIABILITY AND PRODUCTION YIELD RATE WITH MINIMAL DAMAGE DUE TO APPLICATION OF MECHANICAL STRESS AND THERMAL STRESS-- is hereby submitted for the Examiner's consideration.

The drawings have been objected to because the description of the layer that is between layer 3 and layer 1 is missing. Actually, there is no physical layer between the stress cushioning layer (3) and the semiconductor element (1). The line used to separate the stress cushioning layer (3) and the semiconductor element (1) is simply the face or surface of the semiconductor element (1) that is included to describe the exposed end face 1(1) of the semiconductor element (1) as shown in FIGs. 1-33. In view of this explanation, Applicants trust that the objection will be withdrawn.

The disclosure has been objected to due to several informalities listed on pages 2-3 of the Office action. Specifically, the Examiner asserts that the term "devicees" is a typographical error, and should be corrected, and the phrase "(pp. 38-64)" should be changed to –(pp. 40-64)–. Actually, the

typographical error as indicated by the Examiner has already been corrected in the Substitute Specification as filed along with the Preliminary Amendment on October 10, 2001. In that Substitute Specification, many other grammatical and typographical errors have been corrected in compliance with USPTO rules. As for reference to the pages of a cited prior art noted by the Examiner, correction has now been made to the Substitute Specification in order to overcome the objection.

Claims 4 and 10 have been objected to under 37 C.F.R. §1.75(c) as being in improper dependency form. In response thereto, claims 4 and 10 have been amended in compliance with the proper format suggested by MPEP §608.01(n).

Claims 2-3 and 6-9 have been objected to because of several informalities. Specifically, the Examiner notes that the term "player" should be changed to –layer–. In response thereto, claims 2-3 and 6-9 have been amended to overcome the objection.

More significantly, claims 1-3 and 5-9 have been rejected under 35 U.S.C. §102(a) as being anticipated by Yukawa, U.S. Patent No. 6,320,267. In support of this rejection, the Examiner asserts that Yukawa '267 discloses a semiconductor device (see cols. 1-12) comprising an IC (14), an electrode pad (16), a stress cushioning layer (20), a lead wire (26), external electrodes (24), a conductor protective layer (32) and a conductor portion (consider portion underneath [of] the ball-shaped terminals 24) (see Figure 1). The Examiner also asserts that Yukawa '267 further teaches the use of a semiconductor element protective layer (12, 18) (see Figure 1).

However, Applicants disagree with the Examiner's assessment of Yukawa '267, and submit that the features of the present invention are not taught or suggested by Yukawa '267. Therefore,

Applicants respectfully traverse the rejection and request the Examiner to reconsider and withdraw this rejection for the following reasons.

Independent claim 1 defines a semiconductor device comprising semiconductor elements supporting IC devices as shown in FIGs. 1-9 which contain at least a stress cushioning layer (3) installed on said semiconductor elements ... and a conductor protective layer (5) installed on said stress cushioning layer excluding extemal electrodes arranged on a lead wire portion, in which these layers have means for forming each end face on an end surface of said semiconductor elements inside a cutting scribe line and exposing a range from the end face on the end surface of the semiconductor elements to an insidc of the cutting scribe line. This arrangement advantageously enables high reliability and production yield rate when the semiconductor wafer is cut into individual devices with no or minimal damage due to application of mechanical stress and thermal stress.

Likewise, independent claim 5 further defines another component, i.e., a semiconductor element protective layer (7) as shown in FIGs. 1–37. Specifically, claim 5 defines a semiconductor device comprising semiconductor elements obtained by cutting a semiconductor wafer having an integrated circuit and an electrode pad formed on one side along a cutting scribe line, a semiconductor element protective layer (7) installed on said semiconductor elements, a stress cushioning layer (3) installed on said semiconductor element protective layer (7), a first opening formed in said semiconductor element protective layer on said electrode pad, a second opening formed in said stress cushioning layer on said electrode pad, a lead wire portion extending to a top of said stress cushioning layer through said first opening and said second opening respectively from said electrode pad, external electrodes arranged on the lead wire portion on top of the stress cushioning layer, and a conductor protective layer (5)

installed on said stress cushioning layer (3) excluding the extemal electrodes arranged on the lead wire portion, wherein the semiconductor element protective layer (7), the stress cushioning layer (3), the lead wire portion, thc conductor protcctive layer (5), and the extemal electrodes have means for forming each end face on an end surface of the semiconductor elements inside said cutting scribe line and exposing a range from the end face on the end surface of the semiconductor elements to an inside of the cutting scribe line.

In contrast to Applicants' independent claims 1 and 5, Yukawa '267 simply discloses the use of a thermoplastic bonding layer on a radiator plate of a semiconductor chip which is excellent in rcliability in endurance. As shown in FIG. 1, the bonding layer 12 is comprised of two layer structure of a thermoplastic film bonding layer 12a having a thickness of 50 μm and a paste bonding layer 12b having a thickness of 30 μm. A stiffener 20 is then used to bond on the radiator platc 10 surrounding the semiconductor chip 14 with interposition of a bonding layer 18.

Clearly, Yukawa '267 does **not** disclosc the subject matter and the specific arrangement of a stress cushioning layer and a conduction protective layer in the manner defined by Applicants' claims 1 and 5 for maximum production yield rate with minimum or no damage when the wafer is cut due to application of mechanical stress and thermal stress.

Nevertheless, the Examiner asserts that the bonding layers 12 and 18 of Yukawa '267 serve as Applicants' claimed "semiconductor element protective layer" and "conduction protective layer". This assertion is incorrect, however. As expressly described by Yukawa '267, the layers 12 and 18 as shown in FIGs. 1-2 arc bonding layers which are completely different from the semiconductor element protective layer as defined in Applicants' claims 1 and 5 both in function and position (configuration).

In particular, the semiconductor element protective layers of Applicants' claims 1 and 5 are formed on the circuit forming plane of the semiconductor element and do not work as bonding layers. In contrast to Applicants' claims 1 and 5, Yukawa '267 discloses the layers in question (i.e. bonding layers) as being provided on the back surface of the semiconductor element.

In addition, the Examiner also argues that the stiffener 20 of Yukawa '267 serves as Applicants' claimed "stress cushioning layer." However, this is also incorrect. As expressly described with reference to FIG. 1 of Yukawa '267, the function of the stiffener 20 is used for heat radiation and maintenance of package strength. Accordingly, the material of the stiffener is the metal, such as SUS and does not achieve any stress cushioning function. As a result, the examiner's understanding of the function of the stiffener of Yukawa '267 cannot be correct.

The rule under 35 USC §102 is well settled that anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. *In re Paulsen*, 30 F.3d 1475, 31 USPQ2d 1671 (Fed. Cir. 1994); *In re Spada*, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990). Those elements must either be inherent or disclosed expressly and must be arranged as in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989); *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 7 USPQ2d 1057 (Fed. Cir. 1988); *Verdegall Bros., Inc. v. Union Oil Co.*, 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987). The corollary of that rule is that absence from the reference of any claimed element negates anticipation. *Kloster Speedsteel AB v. Crucible Inc.*, 793 F.2d 1565, 230 USPQ2d 81 (Fed. Cir. 1986).

In the present situation, Yukawa '267 fails to disclose and suggest Applicants' claims "protective layers" and "stress cushioning layer" in an arrangement as defined in claims 1 and 5. Therefore,

Applicants respectfully request that the rejection of claims 1 and 5 and all their respective dependents be withdrawn.

Lastly, claims 4 and 10 have been rejected under 35 U.S.C. §103 as being unpatentable over Yukawa, U.S. Patent No. 6,320,267, as modified to incorporate selected features from Johnson, U.S. Patent No. 5,888,849. Applicants respectfully traverses the rejection primarily for the same reasons discussed against Yukawa '267, and also in view of the fact that any proposed incorporation of Johnson '840 will not arrive at Applicants' claims 4 and 10.

In addition, Applicants also submit that Johnson's stiffener does not correspond to the stress cushioning layer of Applicants' claims 4 and 10. In Johnson '840, the stiffener merely serves for maintaining the package strength and does not serve for providing cushion against stress. The reason why the taper is provided for the stiffener is purely for facilitating of production. Namely, unless the taper is provided in the stiffener, it cannot be removed from the mold for transfer molding. Furthermore, in Johnson '840, the stiffener is provided around the semiconductor element. In other words, the stiffener of Yukawa '267 is not formed on the semiconductor element.

In view of the foregoing deficiencies of the proposed combination of Yukawa '267 and Johnson '840, Applicants respectfully request that the rejection of claims 4 and 10 be withdrawn.

Claims 11-20 have been newly added to alternatively define Applicants' disclosed invention over the prior art of record. These claims are believed to be allowable at least for the same reasons discussed against all the outstanding rejections of the instant application.

In view of the foregoing amendments, arguments and remarks, all claims are deemed to be allowable and this application is believed to be in condition to be passed to issue. Should any questions

remain unresolved, the Examiner is requested to telephone Applicants' attorney at the Washington DC area office at (703) 312-6600.

No fees have been incurred. Please charge any shortage in the fees due in connection with the filing of this paper, to Deposit Account No. 01-2135, and please credit any excess fees to such deposit account.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

Hung H. Bui (Reg. No. 40,415)
Attorney for Applicant(s)

HHB:srm
(703) 312-6600

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SUBSTITUTE SPECIFICATION

Paragraph beginning at line 7 of page 3 has been amended as follows:

On the other hand, recently, in association with wide spread use of portable information terminals, there is an increasing demand for miniaturization and high density assembly of a semiconductor device. Therefore, recently, a CSP (chip scale package) having a package size that is almost equal to the chip size has been developed; and, for example, various types of CSPs are disclosed in "Nikkei Microelement" [~~(pp. 38-64)~~] (pp. 40-64) issued by Nikkei BP, Ltd. (February 1998). CSPs disclosed in this publication are manufactured in such a way that semiconductor elements cut into pieces are bonded onto a polyimide or ceramics substrate on which a wiring layer is formed, and then the wiring layer and semiconductor elements are electrically connected, such as by wire bonding, single point bonding, gang bonding, or bump bonding, and the connections are sealed with resin, after which external terminals such as solder bumps are formed thereon.

IN THE CLAIMS:

Please **amend** claims 1-10, and **add** claims 11-20, as follows:

1. (Amended) A semiconductor device comprising semiconductor elements obtained by cutting a semiconductor wafer having an integrated circuit and an electrode pad formed on one side along a cutting scribe line, a stress cushioning layer installed on said semiconductor elements, a lead wire portion extending from said electrode pad to a top of said stress cushioning layer through an

opening formed in said stress cushioning layer on said electrode pad, external electrodes arranged on said lead wire portion on [~~said~~] top of said stress cushioning layer, and a conductor protective layer installed on said stress cushioning layer excluding said external [~~electrode~~] electrodes arranged on said lead wire portion [~~and on a conductor portion~~], wherein said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes have means for forming each end face on an end surface of said semiconductor elements inside said cutting scribe line and exposing a range from said end face on said end surface of said semiconductor elements to an inside of said cutting scribe line.

2. (Amended) A semiconductor device according to Claim 1, wherein said end face of said conductor protective [~~player~~] layer is formed inside said end face of said stress cushioning layer.

3. (Amended) A semiconductor device according to Claim 1, wherein said end face of said conductor protective [~~player~~] layer is formed outside said end face of said stress cushioning layer.

4. (Amended) A semiconductor device according to any one of Claims 1, 2, and [~~to~~] 3, wherein an end area of said stress cushioning layer is formed so as to become [~~taperingly~~] tapered and thinner toward [~~the~~] said end face of said stress cushioning layer.

5. (Amended) A semiconductor device comprising semiconductor elements obtained by cutting a semiconductor wafer having an integrated circuit and an electrode pad formed on one side along a cutting scribe line, a semiconductor element protective layer installed on said semiconductor elements, a stress cushioning layer installed on said semiconductor element protective layer, a first opening formed in said semiconductor element protective layer on said electrode pad, a second opening formed in said stress cushioning layer on said electrode pad, a lead wire portion extending to a top of said stress cushioning layer through said first opening and said second opening respectively from said electrode pad, external electrodes arranged on said lead wire portion on [~~said~~] top of said stress cushioning layer, and a conductor protective layer installed on said stress cushioning layer excluding said external [~~electrode~~] electrodes arranged on said lead wire portion [~~and on a conductor portion~~], wherein said semiconductor element protective layer, said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes have means for forming each end face on an end surface of said semiconductor elements inside [~~a~~] said cutting scribe line and exposing a range from said end face on said end surface of said semiconductor elements to an inside of said cutting scribe line.

6. (Amended) A semiconductor device according to Claim 5, wherein said end face of said conductor protective [~~player~~] layer is formed inside said end face of said stress cushioning layer.

7. (Amended) A semiconductor device according to Claim 5, wherein said end face of said conductor protective [~~player~~] layer is formed outside said end face of said stress cushioning layer.

8. (Amended) A semiconductor device according to Claim 6 or Claim 7, wherein said end face of said semiconductor element protective [~~player~~] layer is formed outside said end face of said stress cushioning layer.

9. (Amended) A semiconductor device according to Claim 6 or Claim 7, wherein said end face of said semiconductor element protective [~~player~~] layer is formed inside said end face of said stress cushioning layer.

10. (Amended) A semiconductor device according to any one of Claims 5, 6, and [~~4 to~~] 7, wherein an end area of said stress cushioning layer is formed so as to become [~~taperingly~~] tapered and thinner toward [~~the~~] said end face of said stress cushioning layer.

--11. A semiconductor device according to Claim 1, wherein said stress cushioning layer is comprised of a pasty polyimide material.

12. A semiconductor device according Claim 1, wherein said stress cushioning layer is made of a low elastomeric material selected from one of fluororubber, silicone rubber, silicon

fluoride rubber, acrylic rubber, silicone fluoride rubber, acrylic rubber, hydrogenated nitride rubber, ethylene propylene rubber, chlorosulfonated polystyrene, epichlorohydrin rubber, butyl rubber, urethane rubber, polycarbonate/acrylonitrile butadiene styrene alloy, polysiloxane dimethyl terephthalate/polyethylene terephthalate copolymer polybutylene terephthalate/polycarbonate alloy, polytetrafluoroethylene, fluorinated ethylene propylene, polyarylate, polyamide/acrylonitrile butadiene styrene alloy, denatured epoxy, denatured polyolefin, and siloxane detnatured polyamide-imide.

13. A semiconductor device according to Claim 5, wherein said stress cushioning layer is comprised of a pasty polyimide material.

14. A semiconductor device according Claim 5, wherein said stress cushioning layer is made of a low clastomeric matcrial selccted from one of fluororubber, silicone rubber, silicon fluoride rubber, acrylic rubber, silicone fluoride rubber, acrylic rubber, hydrogenated nitride rubber, ethylene propylene rubber, chlorosulfonated polystyrene, epichlorohydrin rubber, butyl rubber, urethane rubber, polycarbonate/acrylonitrile butadiene styrene alloy, polysiloxane dimethyl terephthalate/polyethylene terephthalate copolymer polybutylene terephthalate/polycarbonate alloy, polytetrafluoroethylene, fluorinated ethylene propylene, polyarylate, polyamide/acrylonitrile butadiene styrene alloy, denatured epoxy, denatured polyolefin, and siloxane detnatured polyamide-imide.

16. A semiconductor device according to Claim 5, wherein said semiconductor element protective layer is made of a material selected from one of polyimide, polycarbonate, polyester, polytetrafluoroethylene, polyethylene, polypropylene, polyvinylidene fluoride, cellulose acetate, polysulfone, polyacrylonitrile, polyamide, polyamide-imide, epoxy, maleic-imide, phenol, cyanate, polyolefin, and polyurethane.

17. A semiconductor device, comprising:

at least one semiconductor element including an electrode pad formed on one side along a cutting scribe line;

a stress cushioning layer formed on said semiconductor element;

a lead wire portion extending from said electrode pad to a top of said stress cushioning layer through an opening formed in said stress cushioning layer on said electrode pad;

external electrodes installed on said lead wire portion on top of said stress cushioning layer; and

a conductor protective layer installed on said stress cushioning layer excluding said external electrodes arranged on said lead wire portion,

wherein said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes include means for forming each end face on an end surface of said semiconductor element inside said cutting scribe line and exposing a range from said end face on said end surface of said semiconductor elements to an inside of said cutting scribe line.

18. A semiconductor device according to Claim 17, wherein said end face of said conductor protective layer is formed inside said end face of said stress cushioning layer.

19. A semiconductor device according to Claim 17, wherein said end face of said conductor protective layer is formed outside said end face of said stress cushioning layer.

20. A semiconductor device according to Claim 17, wherein an end area of said stress cushioning layer is formed so as to become tapered toward said end face of said stress cushioning layer.